Feasibility Study of MEMS-Based Accelerator Grid Systems for Micro-Ion Engines: Electric Breakdown Characteristics

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Low-temperature (LTO) chemical vapor deposited (CVD) silicon dioxide was investigated for use as an insulator material in microfabricated ion engine accelerator grids. Both substrate (bulk) as well as surface breakdown experiments were performed. Oxide thicknesses for substrate breakdown tests ranged between 1 μm and 3.9 μm. Surface breakdowns were performed over gap distances ranging between 5 μm and 600 μm. Substrate breakdown strengths up to 600-700 V/μm were measured, allowing for maximum stand-off voltages of 2500 V. A slight decrease in breakdown field strength for larger thicknesses was observed. Temperature effects on substrate breakdown field strengths do exist, however, are small. Only a 15% drop in breakdown field strength was noted at 400 C vs. strengths measured at room temperature. Surface breakdown field strengths ranged as high as 260 V/μm , leading to a stand-off capability of 700 V over a 5 μm oxide film. Tests were performed to study the influence of silicon oxide surface morphology on the surface breakdown strength and none was found.

I. INTRODUCTION

dielectric strength

A strong interest has arisen recently within the aerospace community to develop micropropulsion devices capable of delivering very small thrust values and low impulse bits while featuring engine sizes and masses orders of magnitude smaller than are available with current technologies[1]. Applications for such devices would span propulsion needs of some of the smallest and largest spacecraft currently being envisioned, ranging from primary and attitude control of microspacecraft, to precise positioning control of spacecraft constellations for interferometry missions, to compensation of solar-pressure induced torques on large inflatable spacecraft. Microspacecraft[2], typically defined as spacecraft having wet masses of a few tens of kilograms, and possibly extending into the sub-kg mass range, are being considered in order to reduce overall

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mission cost by reducing the mass of the spacecraft. Since launch costs may contribute as much as 30 % to the cost of a mission, microspacecraft will be more cheaply to launch, thus allowing for more frequent access to space. Microspacecraft may also be deployed in fleets or constellations, charting entire regions of space, and reducing mission risk by not relying on a single craft.

However, microspacecraft require radically new approaches in design, both on the system as well as component level. While significant progress in that direction is being made in the instrument, attitude sensing, as well as data handling and storage areas, for example, propulsion still appears to be lacking in this regard, offering only limited hardware choices able to fit the design constraints imposed by microspacecraft with respect to mass, size as well as power[1]. Virtually all propulsion subsystem areas, such as attitude control, primary propulsion and feed system components, are still in need for suitable design solutions. Within the primary propulsion area high specific impulse options may be of particular interest, since their ability to conserve considerable amounts of propellant mass may have a significant bearing on microspacecraft design.

Other space applications, such as the aforementioned interferometry-class or space inflatable spacecraft also may have a need for small, light-weight engine technology able to provide a continuous, low level thrust to offset solar-pressure induced disturbance torques, for example. Depending on the mission, these thrust levels may range from as little as a few mircro-Newtons[3] to a few milli-Newtons. Again, due to the fairly long durations of thrust required over the course of the missions in some of these applications, high specific impulse devices may be desirable.

Currently among the most mature high-specific-impulse (Isp) propulsion technologies is ion propulsion, as evidenced by the recent flight of this technology on NASA's Deep Space (DS) 1 mission. Presently available engine technology, however, is relatively large, extending from beam diameters of 30 cm in case of the DS-1 engine, down to about 10-cm, and requiring power levels on the order of several thousands to several hundreds of Watts[1]. Thus, there obviously exists a need to further miniaturize this technology to make it more amenable to the aforementioned mission categories. Other competing thruster options, such as Field Emission Electric Propulsion (FEEP) and Pulsed Plasma Thruster (PPT) technologies exist and also have reached very high levels of maturity up to the point that one or both are expected to play a role in the types of mission applications discussed[3]. However, micro-ion engine technology, if it can be successfully developed, will be characterized by a unique combination of high specific impulse capability, the use of inert, non-contaminating propellants, lower thrust-to-power ratios than obtainable with FEEP systems, for example, and, unlike the inherently pulsed PPT devices, a continuous mode of operation.

At the Jet Propulsion Laboratory (JPL) there is currently underway a feasibility study to investigate the potential of reducing ion engine sizes dramatically below current state-of-the-art levels. Engine diameters in the 1-3 cm range and thrust levels in the sub-mN to few mN range are being targeted. In order to arrive at a functional ion engine of this small a size, several feasibility issues will need to be investigated and overcome. Among these are the sustainability and efficient operation of high surface-to-volume ratio plasma discharges, the replacement of hollow-cathode technologies with lower-power consuming and easier to miniaturize cathode systems, such as field emitter array technology[4], to function as engine cathodes and neutralizers, and miniature accelerator grid system fabrication and operation, as well as the feasibility of fabrication and operation of miniaturized power conditioning units and feed system components.

In this paper, the feasibility of microfabricated grid designs will be investigated from the perspective of obtainable grid breakdown voltages.

II. MICROFABRICATED GRID DESIGN ISSUES

Although the targeted micro-ion engine diameters of 1 -3 cm are such that microfabrication technologies may not be needed to machine the engine body, a case can be made to investigate the feasibility of microfabricated grid designs. Smaller diameter engines allow grids to be spaced much more closely with respect to each other since the amount of electrostatic-stress induced grid deformation, as expressed by the height of the resulting dished contour of the grids, will be less. Placing grids closer with respect to each other will increase the grid perveance, proportional to $1/d^2$, with d being the grid spacing. Thus, higher beam currents could be extracted form the engine for a given voltage, extending its performance range. However, ion optical considerations generally require grid aperture diameters to be scaled down in size with the grid spacing in order to avoid ion impingements on grids causing potentially engine life threatening erosion, for example. Smaller aperture diameters, and the requirement to place grid apertures of the various grids (screen, accelerator, and, potentially, decelerator grid) of a grid system concentrically with respect to each other, requires tight machining tolerances. Even current grids are machined within 0.05 mm, or 50 μm tolerances, representing a limit in most cases for many conventional machining techniques typically used in grid fabrication, such as electric discharge machining or laser drilling for example. Using microfabrication techniques, however, much smaller tolerances can easily be obtained. In addition, the ability to produce entire batch-fabricated grid systems, not requiring any additional assembly and grid alignment procedures, weighs in favor of microfabrication techniques as well .

In this paper, the feasibility of grids based on silicon-based MEMS (Microelectromechanical Systems) machining techniques is being explored. While other microfabrication possibilities exist, silicon MEMS techniques were investigated first due to considerable heritage and experience available with these technique, as well as its demonstrated ability to produce extremely small feature sizes within very tight tolerances of 1 μm or less. However, MEMS-fabrication of accelerator grids opens up a host of fabrication and operations-related issues. Foremost among them is the selection of appropriate grid materials, suiting both microfabrication as well as grid operation needs, in particular with respect to sputter erosion and voltage stand-off characteristics. In particular the grid insulator material, isolating the screen and accelerator voltages from each other, will have to be able to stand off voltages on the order of 1.3 kV or more over distances on the order of a few micrometer if current grid voltages, and engine specific impulses, are to be maintained, as is desirable.

It is the scope of this study to investigate the feasibility of silicon dioxide as a grid insulator material. Silicon oxide was chosen since it exhibits good electric insulating characteristics when compared to other materials used in silicon-based MEMS fabrication, and is already widely used in the microfabrication field. In order to study the suitability of silicon oxide for this application, both bulk electric breakdown characteristics, as well as electric breakdown characteristics along its surface need to be studied. This is evident when inspecting Fig. 1. As can be seen, both modes of electric breakdown, substrate (or bulk) and surface, are possible in a typical grid design. The latter may occur along the walls of grid apertures. Two experiments were conducted using specially designed silicon oxide breakdown test chips to systematically study both modes of electric breakdown, and will be described in detail below.

The here performed measurements can only be regarded as a first step in evaluating MEMS-based grid designs. Besides the always existing possibility that other insulators, deposited in newly modified and previously untried processes, may result in different breakdown characteristics, one of the most important feasibility issues with respect to grid designs such as the one shown in Fig. 1 is the possibility of coating the insulator material along the exposed grid aperture wall surfaces with conducting, sputter-deposited material. Shadow-shielding around grid spacers is commonly used in grid system today, and similar concepts will need to be explored for microfabricated grids, and to be integrated into the batch fabrication process. However, insulator grid breakdown characteristics were regarded as a logical starting point for a MEMS grid feasibility investigation to be followed up, if successful, in later studies by topics of considerably higher degrees of complexity in fabrication, such as insulator shielding.

II. PREVIOUS RELATED RESEARCH

It may seem surprising at first that a detailed study of breakdown behavior of oxide films is necessary since a substantial amount of research has already been performed in this area over the past decades. However, a closer examination of the available literature reveals that results obtainable from past research may not be directly applicable to the problem studied here.

Most previous research work on breakdown characteristics has been focused on studying the electric breakdown of gate oxides in MOSFET (Metal-on-Silicon Field Effect Transistor) applications. These gate oxides are typically very thin, less than one tenth of a micron thick, and the required minimum breakdown voltages range into the tens of volts, and thus are significantly lower than the kV-voltage range considered for grid applications. One particular type of oxide most frequently considered for gate oxide applications is thermal oxide. This oxide layer is created by directly oxidizing the silicon surface in an oxygen furnace (dry oxide), sometimes aided by the addition of steam (wet oxide) to increase film growth rates[5].

Studies on breakdown strengths of thermal oxides have been performed by Osburn and Ormond[6,7], Osburn and Weitzmann[8], Klein[9], Chou and Eldridge[10], Soden[11], Fritzsche[12], Worthing[13] and Yang et al.[14]. Typically two types of breakdowns were observed by all researchers: the so called primary and the intrinsic, or final, breakdown. Primary breakdown field strengths range from approximately 200 V/μm to as high as 1000 V/μm, whereas final breakdowns follow a more sharply peaked distribution ranging between approximately 800 - 1000 V/μm[6]. In some cases, final breakdown strengths as high as 1400 - 1500 V/μm have been observed for extremely thin oxides[7]. Primary breakdowns are thought to be triggered by thermal instabilities along defects in the oxide[9]. As resistance is locally increased at these defect sites, conductivities locally decrease and the resulting increase in current adds heat dissipation, leading to a further decrease in conductivity, and so on, until breakdown occurs. Using very thin electrodes (less than 0.3 μm in the case of Osburn's and Ormond's experiment[7]) the electrode will be destroyed through evaporation of electrode material near the breakdown location, thus representing a "self-healing" breakdown since no electrical contact can be maintained between the two electrodes due to the loss of conductive material. This allows all defect related breakdown sites to be eliminated until the intrinsic, or final, breakdown is reached. This breakdown strength thus corresponds to the dielectric strength of ideal, defect-free oxide material. Different theories evolve around this final breakdown and both thermal breakdown[9], similar to the process thought to govern defect-triggered breakdowns, as well as electronic breakdowns[7] due to

electron avalanches have been proposed. Chou and Eldridge[10] have succeeded in fabricating virtually defect free thermal oxides and eliminated primary breakdowns, resulting in final breakdown strengths of 600-700 V/μm and up to 1000 V/μm for thermal oxide coated with phosphorsilicate glass, filling pits in the oxides which were believed to have triggered breakdowns.

While it thus appears possible to achieve rather high electric breakdown strengths using carefully prepared thermal oxides, absolute voltages that can be stood off with these oxides may, however, be rather limited. This is largely due to the fact that thermal oxides are typically grown only up to thicknesses of around 1 μm, possibly somewhat larger, but typically always less than 2 μm. The reason for this limitation can be found in the thermal oxidation process. The surface is oxidized directly, i.e. no oxide layer is deposited onto the silicon surface, and the oxide layer instead grows partly into the silicon, using the substrate silicon to form the oxide[5]. Since new oxygen arriving at the surface now has to penetrate an increasingly thicker oxide layer to form an oxidation reaction with the underlying silicon, diffusion limitations will eventually occur, resulting in increasingly larger process times until the process becomes impractical. Therefore, even using Chou's and Eldridge's[10] values for defect-free oxides, the obtainable voltages that can be stood off for oxides being less than 2 μm thick may thus be somewhat marginal assuming that voltages of 1.3 kV will be required for grid applications and an adequate additional margin of safety will have to be maintained.

If, as was the case in most of the experiments conducted, much lower voltage primary breakdowns occur, stand-off voltages would be insufficient for ion engine grid applications. The process of "self-healing" breakdowns, while appropriate in the conduction of experiments addressing fundamental research, would not be suitable for operational ion engine grids since the massive erosion of thin electrode material would lead to grid destruction. In addition, thermal oxides will need to be grown directly on silicon surfaces, thus limiting the choice of substrate materials to silicon only. Although silicon can be doped to render it electrically conductive, other considerations, such as the all-important sputter yield considerations in view of ion engine grid lifetimes, may make this too limited a choice.

Other oxides that have been investigated in the past are RF-sputter deposited oxides. These oxides can be grown to much larger thicknesses (several microns) since the silicon surface is coated with externally supplied, sputter-eroded silicon oxide material. Limitations with respect to thickness arise eventually as thick oxides develop intrinsic compressive stresses which may lead to delamination of oxide from its substrate material. Pratt[15] performed dielectric strength measurements on RF-sputter deposited oxides, however, given targeted applications in the electronics industry, focused only on

very thin oxides. Measured dielectric strengths ranged from 1000 V/μm at 0.07 μm to about 220 V/μm at 0.7 μm. This trend of decreasing electric breakdown field strength is noteworthy and has also been noted for thermal oxides. While breakdown voltages typically still increase with increasing oxide thickness, the trend towards lower electric breakdown field strengths for thicker oxides limits the voltage stand-off capability. In the case of Pratt's experiment, the breakdown voltage at 0.7 μm can thus be calculated to about 150 V.

Klein and Gafni[16] reported electric breakdown field strengths for vapor-deposited oxide films on glass slides, fabricated by evaporation of silicon monoxide in an oxygen atmosphere. Silicon dioxide and silicon monoxide layers were created. The silicon dioxide layers were up to 0.49 μm thick and yielded breakdown strengths of 490 V/μm, or about 250V voltage stand-off capability. Silicon monoxide layers of up to 5 μm were deposited and resulted in electric breakdown field strengths of 192 V/μm, thus yielding a voltage stand-off capability of just under 1000 V. Silicon monoxide breakdown field strengths were found to be lower than those for silicon dioxide for comparable oxide thicknesses. Again, as in the case of thermal and sputter-deposited oxides, a trend towards lower breakdown field strengths with increasing oxide thickness could be noted.

The survey of the literature thus established the need for a more targeted investigation of thick oxides capable of delivering stand-off voltages comparable to typical grid voltages with acceptable margins of safety. Chemical vapor deposited (CVD) oxides are known to produce good electric insulation and can be deposited to thicknesses up to about 5 μm. While some breakdown data can be found in the literature, they very often do not give film thicknesses, or list data for relatively thin films only given the present focus of applications in the semiconductor electronics field. More detailed information was required especially concerning breakdown characteristics of thick oxide films, surface breakdown data, as well as temperature dependence of the breakdown strength of these oxides since grid operating temperatures may range between 300 - 400C.

Therefore, a systematic study of breakdown strengths of LTO-CVD oxides was initiated. Preliminary results were reported in an earlier paper[17]. Those tests were conducted with a limited amount of test chips and thus provided only a very preliminary data base. Although tests in Ref. 17 were initially only targeted to provide substrate, or bulk, electric breakdown field strengths, and tests were therefore conducted in atmosphere for simplicity, unintended electric breakdowns along the

surface were also noted during those experiments. Surface electric breakdown field strengths at the gap distances encountered (about 200 μm) were low, ranging only around 2V/μm. This necessitated a further development of this experiment. First, test chips intended for the measurement of substrate breakdowns had to be redesigned to eliminate the parasitic surface breakdowns, and a more systematic examination of surface breakdowns had to be initiated. The latter tests were to be conducted under vacuum conditions to eliminate any gas breakdown or surface contamination effects. The following section will describe this new set of experiments in detail.

III. DESCRIPTION OF EXPERIMENT

The experiments (substrate, or bulk, and surface breakdown) were conducted with two types of test chips. A total of about 200 chips has been tested. About 100 substrate and 100 surface breakdown tests have been conducted. The chip type used for substrate breakdown is shown in Fig. 2. Each chip is 1 x 1 cm^2 in size. It consists of a silicon substrate wafer (400 μm thick) onto which a thin layer (0.3 μm) of doped polysilicon is deposited (about 22 Ω/□ resistivity). Next a layer of LTO oxide, using a low pressure CVD (LPCVD) silane/oxygen process, is deposited up to a thickness of 3.9 μm at around 450C. Poly and oxide deposition was performed at the University of Berkeley. Some chips tested were poly and oxide-deposited at the University of California/Los Angeles (UCLA) earlier using a similar process, yielding oxide thicknesses of a maximum of 2.7 μm. The latter type of chips was also used in previous tests reported in Ref. 17.

Depending on the desired oxide thickness, the oxide layer is etched back. Next, a via is etched into the oxide to provide access to the polysilicon layer, which will form one of the two electrodes. Finally, a 0.25 μm thick aluminum layer is deposited onto the chip, patterned and etched to form the second electrode as well as a heater coil. This (square-shaped) heater coil can be seen in Fig. 3 and is used to heat the chip for breakdown testing at elevated temperatures. Temperatures up to 400 C have been achieved with this design at power levels of about 11 W (160 V, 0.07 mA). Small variations in heater coil performance were found from chip to chip.

The substrate breakdown tests were performed under atmospheric conditions by placing the test chips into a specially designed quartz fixture, which in turn was placed underneath an IR camera (see Fig. 4). The IR camera was used for temperature measurements and was also able to record arcing on the chip at ambient temperature. The IR image was recorded on video tape for later test

evaluation. The chip was contacted via a probe station featuring four adjustable probe tips. Two tips served as high-voltage leads while the remaining two were used to contact the heater coil. Unfortunately the range of the probe tips was not large enough to test entire wafers. Therefore, wafers had to be diced into individual chips and the chips were tested one by one.

The design of the surface breakdown test chip varied slightly from substrate breakdown chip design. The surface breakdown chip design is shown schematically in Fig. 5. The chip is of the same size as the substrate breakdown chip and very similar in appearance to the chip in Fig. 3, however, featuring smaller contact pad areas. In the case of the surface breakdown test chip, no doped polysilicon layer was deposited onto the silicon substrate. Instead LTO oxide (same process as described above) was deposited directly onto the substrate wafer. Following was an aluminum deposition (same thickness as above), and pattern and etching of the aluminum. Aluminum pads were placed between 100 μm and 600 μm apart, in 100 μm increments. Later in the course of the experiment it was found that testing of molybdenum contact pads was considered desirable, and accordingly chips featuring contact pads made from this material were fabricated. Pads on that set of chips were separated by 5, 10, 20, 100, 200, and 300 μm, respectively, taking into account new data found with the previoulsy described aluminum chips, indicating much higher surface breakdown strengths than measured in earlier tests.

In order to simplify the fabrication process, the surface breakdown test chips also featured a 3.9 μm thick oxide which allowed the wafers to be fabricated in the same oxidation run as the wafers bound for substrate breakdown chip fabrication. In the course of the tests it was noted that the thick oxide had suffered localized surface delaminations in the shape circular, droplet shaped protrusions due to the high intrinsic stresses in the thick oxide. Since it was uncertain how these delaminations would affect surface breakdown strengths, another set of surface breakdown chips featuring a 2 μm thick oxide layer, free of surface delaminations, was also fabricated, and tests were performed with both set of chips to determine the effect of surface morphology on surface breakdown characteristics.

The surface breakdown chips were mounted into a different probe station, also featuring four probe tips, that could be attached to a Scanning Electron Microscope (SEM) vacuum stage (see Fig. 6). Pressures as low as 1×10^{-6} Torr could be obtained, although the majority of tests was performed at around 3×10^{-5} Torr, measured using the SEM stage pressure gage, since this pressure level could be reached rather quickly using the existing pumping facilities. The vacuum stage of the SEM was turbomolecular pumped.

Both breakdown experiments, substrate and surface, were conducted using a portable DC Hypot device by Associated Research, Inc (Model 5220A). This device is capable of delivering up to 15 kV voltage at currents of 2 mA or less. Voltages were recorded with a separate voltmeter (Simpson 260 Series 4). Currents were registered on the scale provided with the Hypot device. This current scale was calibrated and known to be accurate within 3-5%. Prior to breakdown of the chips, however, it was noted that most of the current registered (in the μA range) was flowing through the voltmeter, as current levels were severely influenced by voltmeter settings. During breakdown, however, currents typically ranged as high as 0.5 mA and voltmeter effects were negligible by comparison.

All chips were cleaned after dicing inside the microfabrication cleanroom facilities in an acetone ultrasonic bath for 10 minutes to remove contaminants and remaining photoresist traces, followed by an isopropyl alcohol rinse to remove remaining acetone residues, followed in turn by a dry, and were finally subjected to an oxygen plasma etch at 200 W for 10 minutes to remove remaining organic residue. The chips were then sealed inside plastic trays. The chips were left sealed inside those trays until the moment of usage, at which time they were subjected to the laboratory environment either for the duration of the test (substrate breakdown), or, in the case of the surface breakdown tests, for the duration it took to install one chip onto the probe station and pump down the system, typically a few minutes.

IV. SUBSTRATE BREAKDOWN TESTS

Oxide Thickness Dependence

Determining breakdown field strength with respect to oxide thickness is crucial in the evaluation of LTO oxides for use in ion accelerator grids. As was seen in Section II, electric breakdown field strengths typically vary with oxide thickness, and simple extrapolation of a breakdown field strength obtained for one oxide thickness to a much different thickness may not be appropriate. Chips with oxide thicknesses of 1, 1.5, 2, 2.7, and 3.9 μm were tested. The breakdown field strengths vs. thickness are plotted in Fig. 7. As can be seen, for the thicknesses studied here a small downward trend in breakdown field strength can be noted with increasing thickness. Breakdown field strengths range between approximately 600 - 750 V/μm at 1 μm oxide thickness to around 600 - 650 V/μm at 3.9 μm. Two data points significantly below those values can be found for

two 3.9 μm chips. These values may likely be due to oxide defects. The curve fit shown in Fig. 7 excludes these two data points. Breakdown voltages can thus be found between 600 - 750 V at 1 μm oxide thickness, approaching 2000 V at 2.7 μm thickness, and reaching values as high as 2500 V at 3.9 μm oxide thickness. Thus it can be estimated that LTO oxide thicknesses of 3 μm or greater are fully sufficient to stand off typical grid operating voltages, as far as substrate breakdown is concerned. Later it will be shown that for the associated surface breakdown for this thickness a different conclusion may have to be drawn.

The data obtained in this study for LTO CVD oxide were compared with data obtained for different oxides from the previously reviewed literature (see Section II). Breakdown field strengths for various oxides at different thicknesses are compared in Fig. 8. As mentioned already in Section II, breakdown field strengths much larger than the ones obtained in this study have been recorded in almost every case found in the literature, however, at much lower oxide thicknesses. This increase in breakdown field strength with decreasing oxide thickness appears to become more pronounced with thinner oxides in all cases, independent of the oxide considered, although numerical values vary from oxide to oxide. Thermal oxide breakdown strengths are particularly remarkable, which is precisely the reason for their extensive use as gate oxides in MOSFET applications. It should be noted, however, that the values listed in Fig. 8 for thermal oxide, taken from Ref. 10, are the aforementioned intrinsic, or final breakdown values, and primary breakdown values due to oxide defects are typically significantly lower.

The value of this investigation becomes evident when plotting the obtained breakdown voltages vs. oxide thickness, as shown in Fig. 9. Due to the availability of thicker LTO oxides, achievable breakdown voltages are much higher for LTO oxides than for any other oxide considered in this comparison. Even if breakdown voltages for thermal oxides were to be extrapolated into the 1 - 2 μm thickness range (roughly the maximum obtainable thermal oxide thickness), obtainable breakdown voltages would be marginal for ion engine grid applications, and LTO oxides, due to their larger achievable thicknesses, will still outperform thermal oxides, as well as all other oxides considered. These results displayed in Fig. 9 thus very clearly validate the necessity of this study.

Temperature Dependence

In Fig. 10 electric breakdown field strengths for a 1 μm thick LTO oxide at various temperatures are shown. Temperatures were varied from ambient (23 C) to as high as 400 C. Typical grid temperatures for conventional (macro-sized) grids range between 300 - 400 C. As can be seen, breakdown field strengths decrease slightly with temperature. At ambient, breakdown field strengths range around 600 - 750 V/μm (and breakdown voltages accordingly around 600 - 750 V for a 1 μm thick oxide sample). At 400 C, the breakdown strength has fallen off to 500 - 650 V/μm, corresponding to a breakdown voltage range of 500 - 650 V. This corresponds to drop in breakdown strength and voltage of about 15%.

Attempts were made to repeat measurements at the more relevant oxide thicknesses of 2.7 μm and 3.9 μm, respectively. However, since these tests were performed under atmospheric conditions for reasons of simplicity and in order to have access to the IR camera, and higher voltages are required to cause breakdown in the thicker oxides, heavy arcing was noted on and above the chip surface. Arcing was noted between different locations on the chip, between probe tips and the chip, as well as between probe tips. The arcing was found to be more pronounced at higher temperatures and may have been due to a Paschen breakdown. Since in the case of the 1 μm sample required breakdown voltages are low, these problems were not encountered. Furthermore, the drop in breakdown field strength, at least for the smaller oxide thicknesses, is so low, and the margins with respect to breakdown strengths for ion engine grid applications for the larger thicknesses so great, that temperature effects are currently not being considered a serious impediment to proper grid function with respect to substrate breakdown.

Visual Post-Test Inspection of Test Samples

Electron microscope scans were taken of various test samples after the breakdown tests to determine their failure mechanisms. Figure 11 shows a typical oxide breakdown. It is located at the edge of the aluminum contact pad area, which is still recognizable in the lower part of the photograph although heavily eroded in the immediate vicinity of the breakdown. Note the relatively large size of this breakdown, extending approximately 30 μm in diameter. Oxide thickness in this case was 2.7 μm. Electric breakdown occurred at 1800 V. The oxide used in this case was of the batch provided by UCLA.

Breakdown at the contact pad edges and contact pad corners by far outnumbered breakdowns at other pad locations. Similar observations were made by Soden[11] during his investigation of the dielectric strength of thermal oxides. Soden attributed this fact to the lack of defects in the oxides. If defects would have triggered a breakdown, one would expect the breakdown sites to be distributed more randomly. The fact that breakdowns instead occur predominantly on contact pad edges and corners are an indication that these may be intrinsic breakdowns, triggered by the higher electric field strength in these regions. Small inhomogenities on the contact pad surface or slight variations in the oxide thickness may trigger breakdown at one particular location along the contact pad edge versus another. The high number of breakdowns observed on contact pad edges leads us to believe that the oxides were mostly free of defects.

Figure 12 shows a side-on view of the breakdown shown in Fig. 11, clearly indicating that the oxide layer, visible as the lightly colored layer just above the darker colored silicon substrate, has been penetrated (the polysilicon layer, being only 0.3 μm thick, is hardly visible on the photograph and appears as a very thin black line just between the silicon substrate and the oxide in the original). As can be seen, besides destroying the oxide layer, substantial damage has also been done to the silicon substrate located directly below the breakdown area, likely due to the substantial local Joule heating during breakdown. Although no temperature measurements on the arc were performed in this study, Klein[9], in performing spectroscopic temperature measurements on the breakdown arc, determined arc temperatures on the order of 3900 - 4500 K for thermal oxide breakdowns. If similar temperatures were to occur in LTO breakdowns as well, these values would certainly be sufficient to melt the silicon substrate, having a melting temperature of about 1400 C.

Figure 13 shows a spectral (X-ray fluorescence) analysis of the distribution of elements surrounding the breakdown shown in Figs. 11 and 12. Three picture segments show the distribution of silicon (top right), aluminum (bottom left) and oxygen (indicative of silicon oxide, bottom right) as seen from a top view position similar to the one shown in Fig. 11. As can be seen by inspecting the top right segment, silicon is clearly visible through the gap in the oxide layer, which shows up as a dark ring shaped structure in the oxygen scan in the bottom right segment, indicating the lack of oxide here. This, together with the visual evidence presented in Fig. 12, also gives a clear indication that a break-through to the underlying silicon/polysilicon layers has indeed taken place. Also visible in these scans is the heavy erosion of the aluminum contact pad (located in the lower half of the picture segments). While some aluminum traces can still be found in this area (see lower left picture segment), the silicon oxide, onto which the aluminum contact pad was deposited, is clearly visible in this area now as well (see lower right picture segment).

In the case shown Figs. 11-13, as in all breakdown cases recorded during this set of experiments, a permanent short was noted after breakdown. Voltages typically collapsed to values ranging around a few tens of volts or less (after having been as high as several hundred or even thousands of volts just prior to the breakdown) and currents in excess of 0.5 mA were measured (current values prior to breakdown were on the order of a few micro-Amps to possibly extended into the low 20 μA range in some cases, but were found to be dependent on the volt-meter setting. It is thus believed that a substantial fraction of this current went through the meter, rather than through the sample). The short is likely caused by the severe disturbances noted in the breakdown area, as seen in Fig. 12, mixing elements of the various chip layers, thus providing electrical contact.

Figure 14 shows another breakdown of a chip featuring 2.7 μm thick oxide, with the breakdown also occurring at 1800 V, as in the case of the chip depicted in Figs. 11 through 13. This chip was fabricated using the oxide provided by Berkeley. A peculiar meandering pattern can be noted on the chip surface in areas that have seen heavy aluminum pad erosion. The sequence of events, as documented by the IR camera and recorded on tape, was as follows: Breakdown first occurred at a contact pad edge location in the top left corner of the pad area. The probe tip contacted the pad area in the location shown. After breakdown at the contact pad edge, the aluminum pad eroded outward from the initial breakdown location, with the eroded aluminum pad edge recessing until it reached the probe tip location. At this point the erosion process stopped. The voltage dropped from 1800 V prior to breakdown (at small μA current values believed to be conducted largely through the volt meter), to about 500- 600 V and about 0.5 mA during the surface erosion/arcing process, and finally collapsing to the aforementioned few to few tens of Volts depending on chip sample at currents of about 0.5 mA, shorting the circuit. Current and voltage values, except for the initial breakdown voltage of course, were found typical for most chips breaking down in this fashion, except for the ones using the thinnest oxides (1 μm - see below).

At first glance, the meandering erosion pattern seems to point to a pure surface breakdown phenomenon as a result of arcing between the - after the initial breakdown at the pad edge - exposed grounded polysilicon layer and the aluminum pad edge which is held at high voltage and which typically evaporates around the initial breakdown area as a result of excessive Joule heat. The surface arcing between the breakdown area and the aluminum layer could then be thought to then continue to generate heat which causes the aluminum layer to ablate further until the probe location is reached,

representing the minimum path of resistance to the high-voltage supply. A more detailed study, however, reveals a more intricate process.

Figures 15 through 17 show a detailed view of the initial breakdown area and the starting point of the meandering "tree-shaped" pattern that was observed on the chip surface. Figures 16 and 17 were obtained by dicing the chip along one of the "branches" of the "tree" pattern. In Fig. 16, the initial breakdown can be seen, revealing a similar structure as the breakdown shown in Fig. 12. Again, a penetration of the oxide layer combined with a significant disturbance of the various layers of the chip (aluminum, oxide, polysilicon and silicon substrate) can be observed. Just to the right of the initial breakdown area seen in Fig. 16, however, along one of the surface breakdown "tree branches", additional penetrations of the oxide and cavities formed inside the silicon substrate can be noted. This pattern continues if one were to progress further to the right of the location shown in Fig. 16, as seen in Fig. 17. Clearly, a large penetration of the oxide can be noted in the left half of Fig. 17. Additional cavities appear to be sealed by the oxide layer, however, it should be noted that dicing further into the chip may have revealed these cavities to be "open" as well, thus quite possibly representing oxide penetrations as well. Thus, the process forming the meandering "tree" pattern on the surface of this chip is clearly not a sole surface phenomenon, but involves subsurface events as well.

Similar erosion patterns have previously been observed by Klein[9] during breakdown tests performed on thermal oxides. Klein termed these types of breakdowns "propagating breakdowns" and offered an explanation for their occurrence. According to Klein[9], the breakdown starts at a single location, as observed in our experiments also. Due to the Joule heat produced by this initial breakdown conductivity of the insulator material may be slightly lowered in the vicinity of the initial breakdown location, causing another breakdown to occur in an area immediately surrounding the initial breakdown location. The process now continues, causing the "tree branch" pattern to form. Since, as was noted in this study, a current of approximately 0.5 mA is constantly flowing between the two electrodes during this erosion process, a (however minute) voltage drop is expected to occur along the uneroded aluminum pad area, extending from a high value at the location of the contacting probe tip to a low value in the proximity of the eroded pad edge. Thus, a preferential direction is given for subsequent breakdowns to occur (towards higher voltage values) until one of the "tree branches" finally connects with the probe tip location. It should be noted that the observed surface erosion process could be stopped anytime after the initial breakdown and the low voltage short would still have been observed, as was demonstrated in various test runs.

Another interesting breakdown pattern can be observed in Figures 18 through 21. Figures 18 and 19 show a chip featuring an oxide thickness of 1 μm after a 750 V breakdown. As can be seen, multiple breakdown locations can be recognized distributed over an area that was again located close to the contact pad edge. Several breakdowns had again occurred very near to this edge. In Figs. 20 and 21 another breakdown of a 1 μm oxide chip is shown. This chip broke down at 750 V also, however, this test was performed at 205 C (all previous chips discussed in this section were tested at ambient temperature, about 23 C). Again, multiple breakdown locations can be noted, many of them close to or on the contact pad area edge, with one breakdown occurring at one corner of the pad (see Fig. 21). All breakdowns again penetrate the silicon oxide layer deep into the silicon substrate and causing the already previously noted severe disturbance of the chip material in this area, again leading to a permanent short after breakdown. Current and voltage characteristics for the shorts in 1μm chips were around 0.3 - 0.4 mA and with voltages ranging mostly around 0.15 V to about 12 V, with one value being as high as 150V. The breakdown patterns shown in Figs. 18 and 20 did not occur instantaneously, but required time to develop, with arcing starting near the edge or corner of the contact pad, and then progressing inward towards the probe tip location. In the case of the chip shown in Fig. 18, this process stopped on its own after reaching the state depicted in the figure. Current and voltage characteristics for these chips during this arcing process were around 0.3 mA and 400 V, and thus, as for the case of the shorts, slightly lower than in the case of thicker oxides.

Again, this type of breakdown pattern has been observed before by Klein[9] in his study of dielectric strengths of thermal oxides and was attributed by Klein to the same thermally triggered breakdown process as described above. However, the different appearances of the two classes of propagating breakdown patterns shown in Figs. 14 and 18 and 20, respectively, warrant a closer examination. One obvious difference between the chips exhibiting these different propagating breakdown behaviors is the much smaller oxide thickness (1 μm vs. 2.7 μm) in the case of the chips shown in Figs. 18-21 vs. the chip shown in Fig. 14. Several tests were performed to examine how breakdown patterns for intermediate oxide thicknesses would appear. The results of one of these tests is shown in Fig. 22. The breakdown pattern exhibited on this chip appears to be somewhat of a cross between the two classes identified above: While multiple, separated breakdowns did occur near the edge, almost all of these breakdowns show rudimentary "tree" growth emanating from the breakdown locations.

We believe an explanation for this behavior may be found in possibly different thermal conduction processes in chips of different oxide thicknesses. Silicon dioxide is a poor thermal

conductor when compared to silicon, the thermal conductivity being 1.4 W/mK in the case of oxide versus about 150 W/mK for silicon. Given that the destruction found underneath the initial breakdown locations involves the silicon substrate, heat conduction away from the initial breakdown site is likely to occur both through the oxide as well as through the silicon. Some portion of the heat will be conducted radially outward directly through the oxide layer, while another portion will be conducted through the silicon and, from positions radially further outward from the initial breakdown location, maybe directed partially back into the oxide layer as this layer is being heated from the underlying silicon substrate. For thinner oxides a larger fraction of heat may thus be received faster at locations further away from the original breakdown location by conduction through the silicon substrate, which in turn could lead to breakdowns further away from the initial breakdown site. Since those locations closer to the high-voltage probe tip will carry the majority of the current as it seeks its path of lowest resistance, the current passing through the original breakdown site may subside and no additional breakdowns in its immediate neighborhood, as shown in Fig. 16, may occur. The ultimate location of the individual breakdowns, apart from the temperature profile, may then be determined by small variations in oxide thickness or inhomogenities on the contact metal surface. Since again a current is constantly flowing between the two electrodes (polysilicon and aluminum), as observed in these experiments, a voltage drop will again extend from the high-voltage probe tip location on the aluminum pad to its eroded edge and thus again provide a preferential direction for further breakdowns, until the position of the high-voltage probe tip has been reached. As in the case of the previously discussed class of breakdowns, it can be stopped immediately after initial breakdown by turning off the voltage.

V. SURFACE BREAKDOWN TESTS

Dependence on Gap Distance

As was noted in the Introduction and indicated in Fig. 1, in an ion engine accelerator grid arcing may also occur along the insulator oxide surface. Previous tests performed by the authors under atmospheric conditions[17] had led to parasitic surface breakdowns when performing substrate breakdown tests. The resulting surface breakdown voltages were a troublesome 2V/μm over gap distances of about 200 to 300 μm. Surface breakdown field strengths that low, if applied over a 5 micron thick oxide layer (corresponding to roughly the maximum LTO oxide thickness that can be deposited), would be wholly insufficient for ion engine grid applications. Thus, a more thorough investigation of surface breakdowns along LTO oxide surfaces was conducted. These tests were

performed in a vacuum system, as outlined in Section III. Unless otherwise notes, breakdown tests were performed at a vacuum pressure of 3 x 10^{-5} Torr.

Given the low measured breakdown field strength in earlier experiments[17], initial tests were performed with contact pads separated by a gap distance of 100, 200, 300, 400, 500, and 600 μm, respectively. Results obtained from these tests are shown in Fig. 23. As can be seen, surface breakdown electric field strengths range from around 20 V/μm at a 100 μm gap distance to as little as 3-4 V/μm at a 600 μm gap distance between the aluminum pads. At values between 200 - 300 μm, electric breakdown field strengths are around 10 V/μm, thus clearly higher than for breakdown under atmospheric conditions.

Even these increased breakdown field strengths, however, were still too low for ion engine grid applications. Suspicions were raised that the use of aluminum, which has a tendency to form hillocks on its surface, may have led to decreased voltage stand-off capability as a result of these surface roughnesses[18]. Aluminum had been used in the design of these test chips because of it being readily available in our cleanroom facilities, ease of use in the microfabrication process, past expansive experience with its use as a MEMS material, as well as good sticking abilities. In addition, Osburn and Ormond[7], in performing experiments aimed at determining substrate breakdown field strengths for thermal oxides, had tested various electrode materials, including aluminum and molybdenum, and had found no difference in breakdown behavior.

To resolve remaining doubts and uncertainties chips using molybdenum contact pads were fabricated. In addition, due to the noted slight increase in breakdown field strength for the chips using aluminum pads, the mask design for the molybdenum chips was changed and now, in addition to gap distances of 100, 200, and 300 μm, included gap distances of 5, 10, and 20 μm to perform tests at these lower gap distances as well. The obtained data are also plotted in Fig. 23 (open squares) and represent the steeply inclined part of the curve. Two remarkable findings are to be noted: First, in testing molybdenum chips at a 100 μm gap distance, it was noted that there is no apparent difference in surface breakdown field strength when compared with chips featuring aluminum contact pads. Data for the 100 μm gap distance for both types of contact pads almost overlap identically at around 20 V/μm. These results obtained for surface breakdown experiments on LTO oxides thus mirrors experiences gained by Osburn and Ormond[7] with substrate breakdowns of thermal oxides.

Secondly, when decreasing the gap distance further, a remarkable increase in breakdown field strength can be noted. At least three measurements were taken for each gap, with results repeating each other with comparably little scatter in data. This increase in surface breakdown field strength towards lower gap distances thus mirrors a similar behavior found for substrate, or bulk, breakdown of many other oxides (compare with Fig. 8). Note that two separate curve fits were used, one for the molybdenum data, another for the aluminum data, yet both curves appear to match very well.

This increase in electric breakdown field strength is encouraging, however, still not quite sufficient for ion engine accelerator grid use, as can be seen by inspecting Fig. 24. For gap distances of 5 μm, representing the approximate maximum LTO oxide thickness that can be deposited, breakdown voltages remain just below 1000 V. Thus, a new approach was explored. A set of surface breakdown test chips was fabricated featuring an oxide undercut extending below the (molybdenum) contact pad (see Fig. 25). The undercut was achieved through a Buffered Oxide Etch (BOE). This undercut was hoped to accomplish (1) an increased breakdown surface path, thus increasing surface breakdown voltages, and (2) eliminate the sharp 90° edge of the pad in direct contact with the oxide, thus hopefully decreasing local field strengths and therefore delaying the onset of breakdown to larger voltages. This chip design was influenced by cold cathode designs. Using similar designs, Spindt[18] has reported breakdown voltages of up to 250 V/μm and more.

Table 1 lists results obtained with a set of chips featuring an oxide undercut as shown. A 5 μm gap was tested. For comparison, data obtained for chips with the same gap distance, but without an oxide undercut were tested as well. Both set of chips were fabricated from the same wafer and were exposed to the same fabrication processes and condition, except for the oxide etch in the case of the chips featuring the undercut. As can be seen by inspecting Table 1, although one single data point obtained for a chip featuring an undercut resulted in a record breakdown field strength of 260 V/μm at 1300 V breakdown voltage, the remainder of the results is not very convincing. As a matter of fact, in some cases the breakdown field strengths and voltages obtained with chips featuring undercuts are lower than those not featuring an undercut, although this may be an effect of the scatter of data. Thus, the undercut does not appear to be effective, at least within the current chip geometries. It is possible that the oxide etch may also affect the molybdenum and may increase surface roughnesses, counteracting any desired effects the change in geometry may have caused, if any. It is interesting to note that breakdown voltages obtainable with cold cathode arrays, featuring similar electrode/insulator

geometries, yields breakdown values as high as 250 V/μm, however, at smaller thicknesses[18]. It is unclear whether breakdown occurs through the substrate or along the surface in these cases.

Paschen Breakdown Considerations

An experiment was conducted to determine the influence any remaining rest gases in the vacuum system might have had on the measurements, if any. In Fig. 26, breakdown voltages are plotted versus the product of gas pressure inside the vacuum system and gap distance. Using this representation, if arcing through the rest gas would have been present, a Paschen-type curve should have resulted. All measurements were performed at a gap distance of 100 μm and pressure was varied by taking measurements at various stages during the pump down process. This allowed for measurements at pressures ranging between 10^{-4} Torr to as low as 10^{-6} Torr. Accordingly, pressure and gap products are extremely low, ranging between 10^{-8} Torr cm to 2 x 10^{-6} Torr cm. Typically, these values would indicate a position far too the left of the minimum of the Paschen curve for commonly used gases that could have been present in the chamber (nitrogen, oxygen, water vapor traces). At these values, if a Paschen breakdown would have been present, breakdown voltages should have been much higher than observed and should have decreased dramatically towards larger pressure and gap product values. In inspecting Fig. 26, however, it is clear that this is not the case. No particular trend is visible among the data points and only the usual scatter of the data, as observed for measurements taken at constant pressure and gap distance as well (see Fig. 24), can be noted. Thus, it was concluded that the surface breakdowns observed were likely true surface effects.

Influence of Surface Morphology

During early surface breakdown measurements, chips fabricated from wafers featuring a thick 3.9 μm oxide were used for reasons explained in Section III. In the course of these experiments it was discovered that droplet-shaped surface features were present on the chip surface, and thus in the gap area as well (see Figs. 27 and 28). Feature sizes ranged between 3 μm (Fig. 27) and less than 1 μm (Fig. 28) in diameter. Naturally, it was feared that these features could have had an influence on the obtained data and be at least partly responsible for the low surface breakdown strengths. It was quickly determined, through a combination of X-ray fluorescence spectral analysis, as well as various standard cleaning techniques, that the surface features were not contaminations resulting from organic residue, photoresist, or else, but, instead, were stress delaminations caused by the large

intrinsic stresses in the thick LTO layer. Consequently, wafers featuring thinner oxides (2 μm) were fabricated and used in subsequent tests.

However, using these chips, an unexpected opportunity presented itself to study the influence oxide surface morphology might have on surface breakdown characteristics. Chips of the original 3.9 μm LTO batch, chips fabricated by UCLA using a 2.7 μm oxide featuring fewer delaminations, as well as the latest Berkeley batch using 2 μm oxide having no detectable delaminations, were tested and data obtained were compared. All surface delaminations inside the gap area were counted under an optical microscope and average surface densities in the gap area were calculated. These densities are believed to be accurate within less than 10% or so, since counting this great a multitude of features lead to miscounts, in particular since in some cases chips had already been tested and debris resulting from aluminum pad erosion had to be discerned from surface delaminations. However, this accuracy is believed to be sufficient, considering that a very wide range of surface delamination densities, ranging from zero to as high as 4000/mm^2 were obtained.

Figure 29 shows the results for three gap distances: 100, 200 and 300 μm. No particular trend of breakdown field strength with respect to delamination density can be observed for either of the gap distances. The scatter in breakdown field data appears somewhat less pronounced for lower delamination densities, but differences remain small. There definitely appears to be no trend towards lower breakdown field strengths at higher delamination densities. Therefore, it was concluded that surface morphology of the type observed in Figs. 27 and 28 did not affect breakdown strengths. However, it should be pointed out that the particular surface features encountered here have relatively smooth shapes and comparably large radii of curvature.

Visual Post-Test Inspection of Test Samples

All surface breakdown test samples appeared very similar after breakdown. Examples of two chips imaged after breakdown are shown in Figs. 30 and 31. Both chips featured aluminum contact pads and a gap distance of 100 μm. Arcing occurred preferentially at the corners of the pad area, but also at straight edge sections. Depending on the intensity of the arcing, usually well correlated with the magnitude of the breakdown voltage, isolated burn marks, as in Fig. 30 (breakdown at 2100V, or 21V/μm), or extensive erosion along the entire pad edge, as in Fig. 31 (breakdown at 3200V or 32 V/μm), can be observed. Damage is typically more intensive on the negative pad (shown in the left of

both Figures) than on the positive pad. It is not certain what the cause for this behavior is. One explanation offered was that electron field emission from microscopic tips along the negative pad edge may have lead to local heating and thus increased erosion. An example of an (uneroded) aluminum contact pad edge can be seen in Fig. 32. Tips protruding from the edge are small (approx. less than a few tenths of microns, representing state-of-the-art microfabrication/patterning technology), however, are sharply pointed. Finally, Fig. 33 shows the eroded negative pad area of a molybdenum pad. Molybdenum thickness was about 0.05 μm and thus the damage was more severe.

VI. CONCLUSIONS

Microfabricated ion accelerator grids are being considered for use in micro-ion engines due to the unrivaled precision with which these components could be built. In particular for grids, requiring a multitude of closely spaced apertures placed within tight tolerances to provide proper grid hole alignment and beam extraction, mirofabrication techniques may be beneficial. However, fabrication of these grids will require the use of new materials, typically not used in the fabrication of conventional grids, requiring an investigation into the feasibility of such an approach.

Among the material properties to be studied is the dielectric strength of grid insulator materials. One of the most popular insulator material used in the MEMS area is silicon dioxide. Most breakdown work in the past however, was focused on the evaluation of thin thermal oxides for use as gate oxides in MOSFETs. While these oxides show excellent electric breakdown field strengths for thin layers, thermal oxide, due to its growth process, can typically only be grown up to thicknesses not exceeding 2 μm. Over these thicknesses, the total voltage that can be stood off is marginal with respect to ion engine grid applications. On the other hand, CVD deposited LTO oxide can be deposited up to thicknesses of possibly 5 μm. However, many details of the dielectric properties of LTO oxides, in particular for very thick films, and at elevated temperatures, were not known. Thus, a thorough investigation of these properties was initiated. Results of this evaluation remain mixed at this point of the investigation.

On the one hand, substrate, or bulk, electric breakdown properties of LTO oxide are excellent. Voltages as high as 2500 V can be stood off over oxide thicknesses of 3.9 μm, providing more than sufficient margins of safety for grid applications. In addition, there are strong indications that the oxides used show little to no defects that could lead to premature electric breakdown as evidenced by the fact that breakdowns usually occurred near contact pad edges, rather than being randomly

distributed as would be expected if defects would have caused these breakdowns. No particularly adverse temperature effects with respect to breakdown strengths were noted for LTO oxides either. Although a small drop in breakdown strength was measured for a 1 μm thick oxide sample, decreases are small (approximately 15%) with increasing temperatures from ambient to 400 C. Breakdown voltages obtained compare very favorably to corresponding literature data found for other oxides, such as thermal and sputter deposited oxides. In the case of thermal oxides this is mainly due to the comparatively larger LTO oxide thicknesses that can be deposited.

On the other hand, surface breakdown properties still appear inappropriate. Although it was discovered that surface breakdown electric field strengths increase significantly with smaller gap distances, reaching values around 200 V/μm for 5 μm, obtainable voltages over these distances remain relatively small (i.e. less than 1000 V). New grid/insulator geometries were therefore explored, based on certain cold cathode design features. Since breakdowns tended to occur predominantly along contact pad edges and near corners, it was reasoned that the field concentration at these locations does play a major role in oxide breakdowns. Chips with oxide undercuts, extending underneath the contact pad edges were therefore fabricated. The maximum obtainable field strength at break down obtained using these chips was 260 V/μm, but in most cases were comparable to results obtained with chips featuring no undercut, rendering the undercut rather ineffective. It is interesting to note that similar electrode/insulator configurations featuring oxide undercuts have been used in cold cathode arrays in the past and resulted in breakdown field strengths of up to 250 V/μm.

Thus, results obtained so far for ion engine grids fabricated using silicon-based MEMS technologies do not look promising. There does exist the possibility to use these types of grids for lighter inert gas propellants than Xenon, such as Krypton or Argon, since required grid voltages will be lower, however, this will impose limitations on propellant selection that may not be desirable. Another possibility that has emerged only recently is the use of very thick PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide films reaching thicknesses up to 15 μm as proposed by ..... Although PECVD oxide films typically do not have the same quality as LTO oxide films, the much larger thickness available with these films may well compensate for any defects, if any. Finally, non silicon-based microfabrciation techniques will also be explored in the near future.

VII. ACKNOWLEDGEMENTS

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Table 1: Surface Breakdown Voltages and Field Strengths fo a 5 μm Gap using Oxide Undercut

Oxide Undercut (5 μm Gap)		**No Oxide Undercut (5 μm Gap)**	
Breakdown Voltage (V)	Breakdown Field Strength (V/μm)	Breakdown Voltage (V)	Breakdown Field Strength (V/μm)
600	120	700	140
600	120	700	140
900	180	700	140
900	180	800	160
1300	260	900	180
		900	180
		950	190

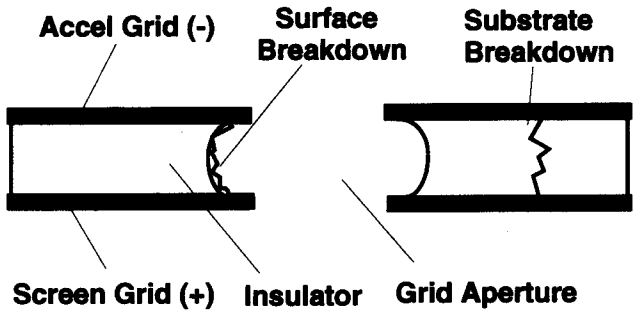

Fig. 1: Anticipated Grid Breakdown Modes

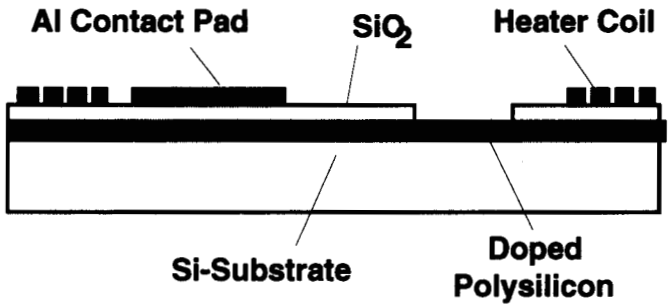

Fig. 2: Schematic of Substrate Breakdown Chip

Fig. 3: View of Substrate Breakdown Test-Chip

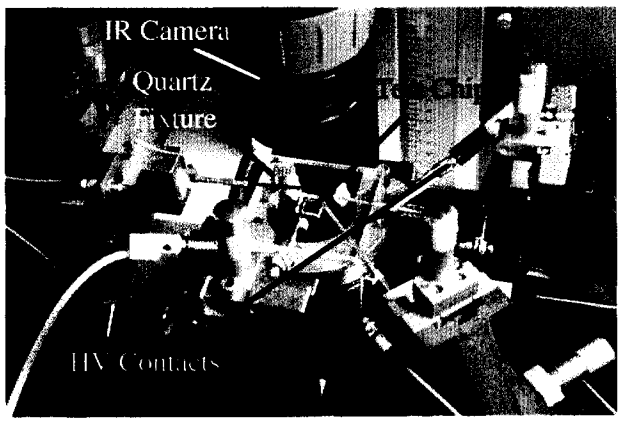

Fig. 4: Substrate Breakdown Test Set-up

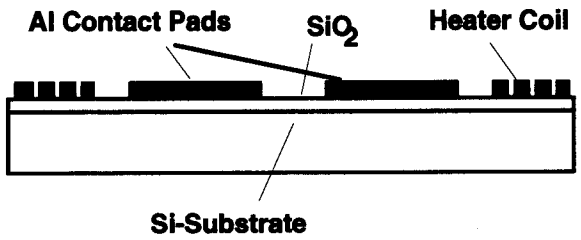

Fig. 5: Schematic of Surface Breakdown Chip

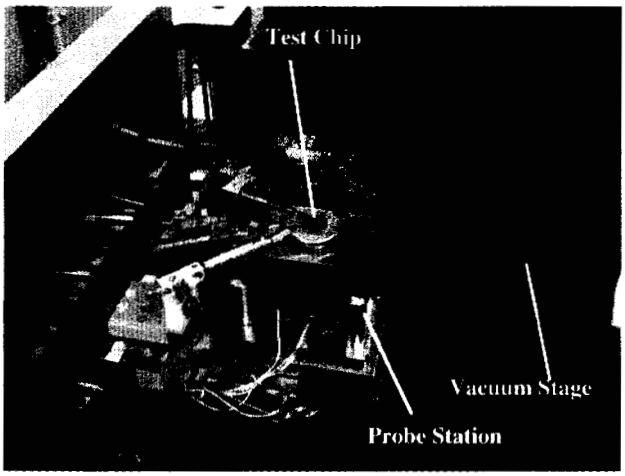

Fig. 6: Experimental Set-up for Surface Breakdown

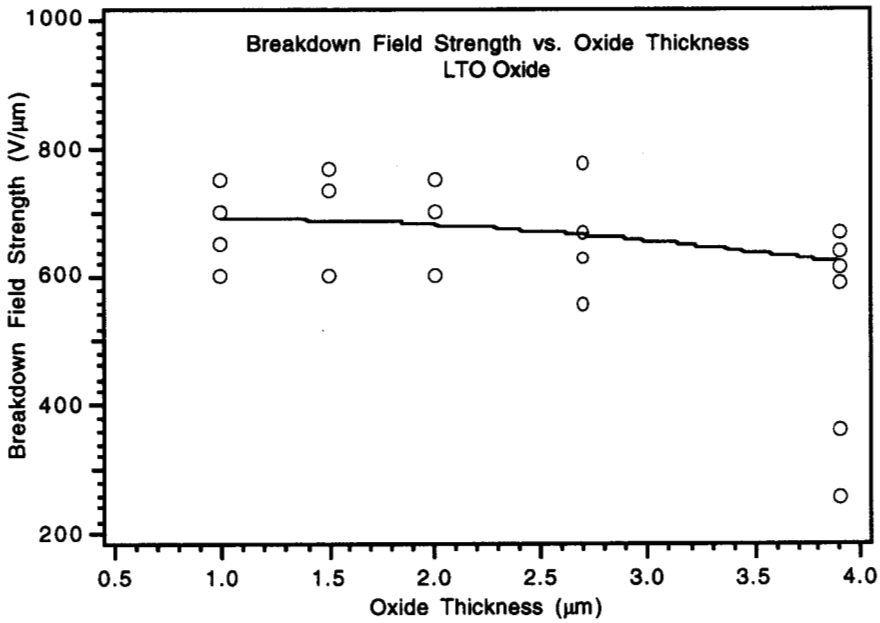

Fig.7: Electric Breakdown Field Strength vs. LTO Oxide Thickness

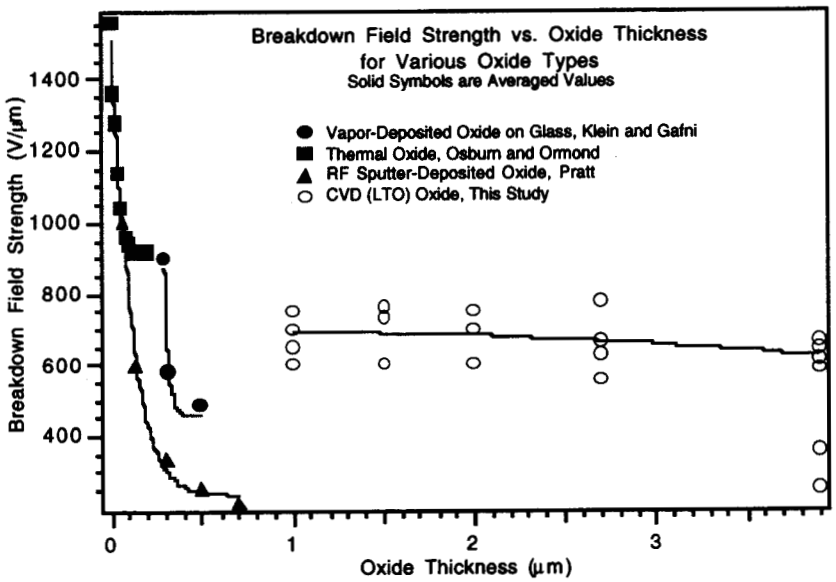

Fig. 8: Breakdown Field Strengths for Various Oxides vs. Oxide Thickness

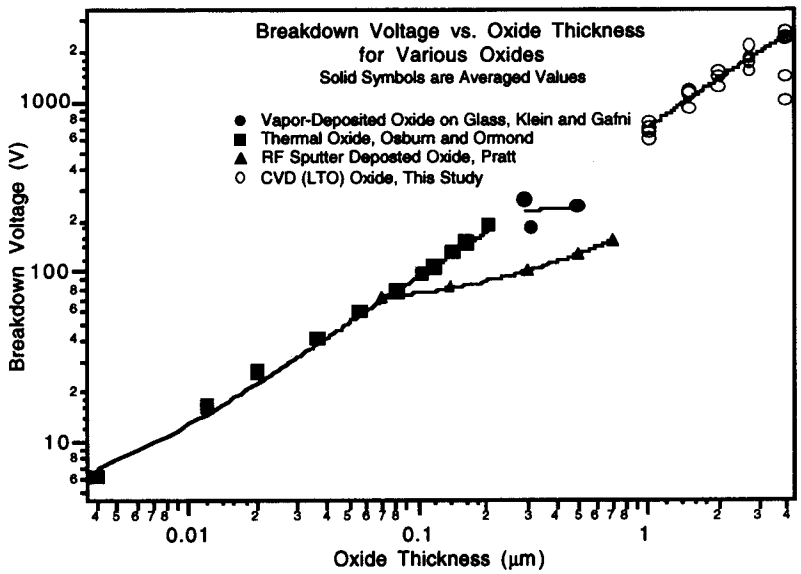

Fig. 9: Breakdown Voltages vs. Oxide Thickness for Various Oxides

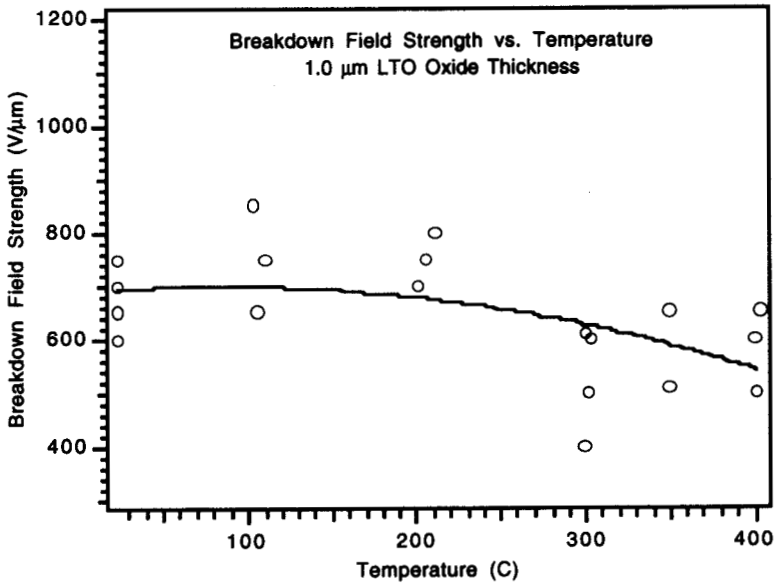

Fig. 10: Electric Breakdown Field Strength vs. Temperature for 1 μm LTO Oxide

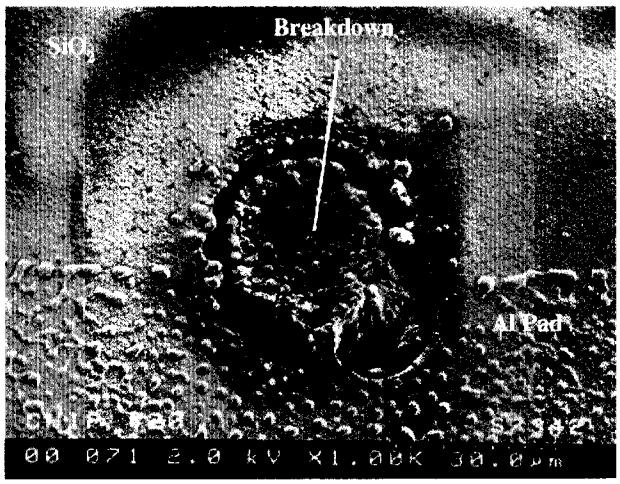

Fig. 11: Electric Breakdown at Aluminum Contact Pad Edge

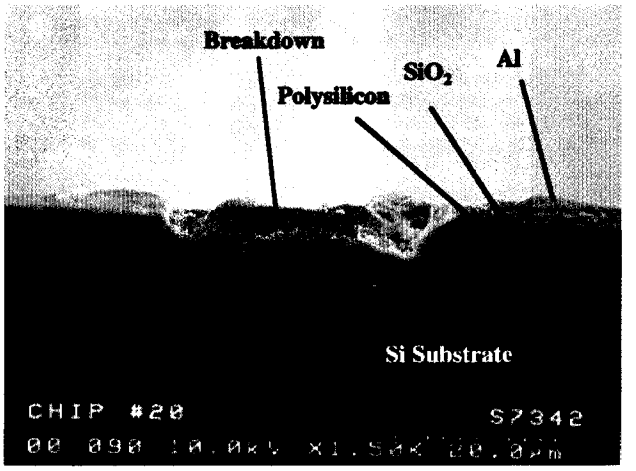

Fig. 12: Side View of Breakdown shown in Fig. 11

Fig. 13: Spectral (X-Ray Fluorescence) Analysis of Breakdown shown in Fig. 11.

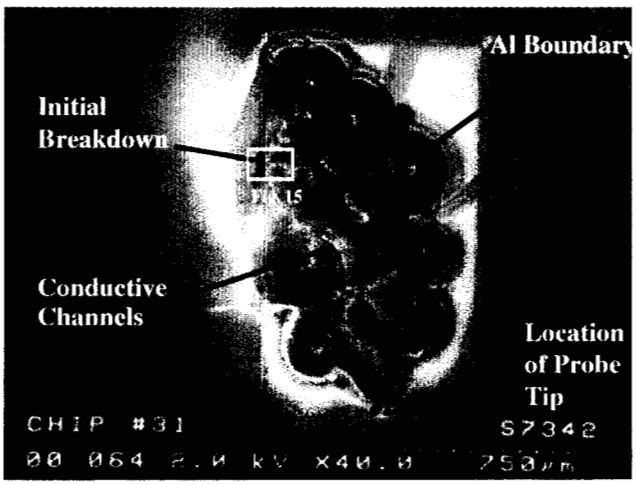

Fig. 14: Propagating Breakdown Pattern showing "Tree- shaped" Conductive Channel Formations

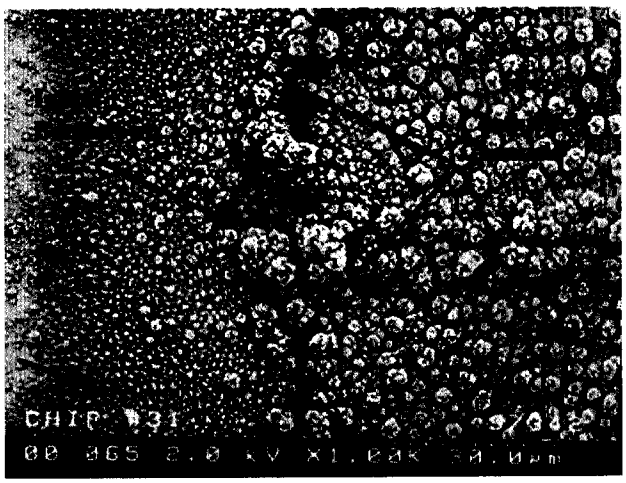

Fig. 15: Close-up of Initial Breakdown Location in Fig.14.

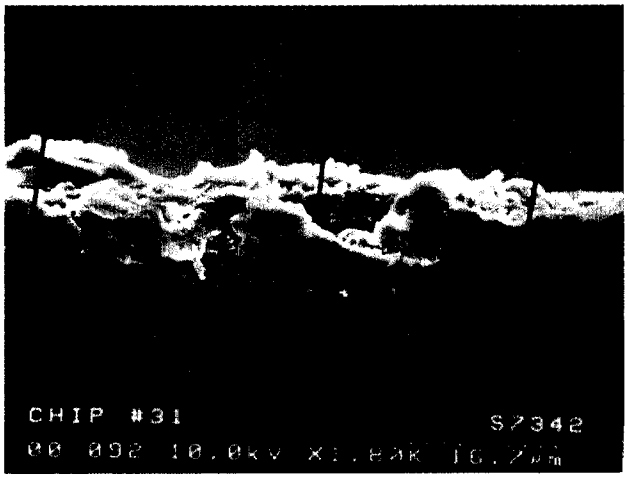

Fig. 16: Side-View of Initial Breakdown Area shown in Fig.15

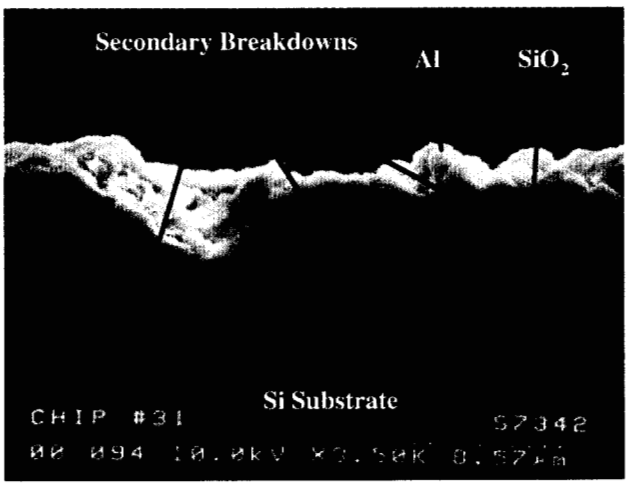

Fig.17: Side-View of Conductive Channel Segment, located to the right of Formation shown in Fig. 16.

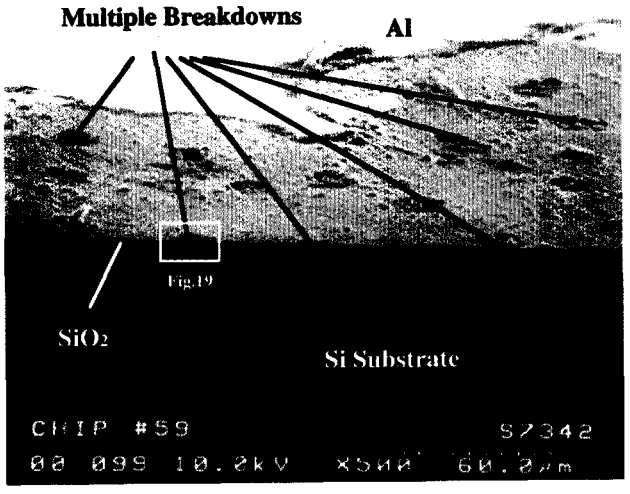

Fig.18: Example of Multiple Breakdown Locations for Thin Oxides (1 μm).

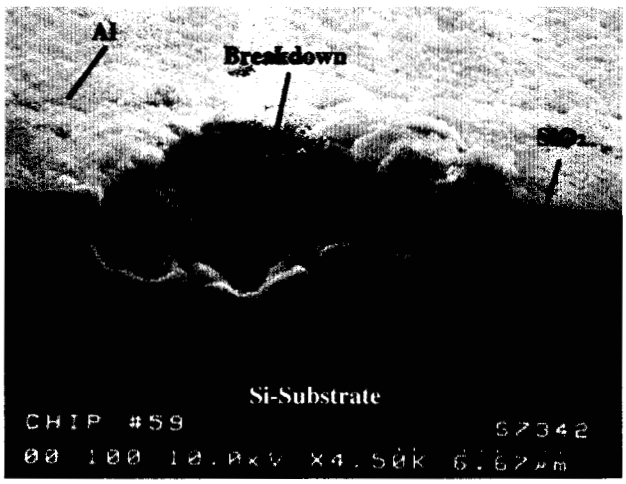

Fig. 19: Close-up of Breakdown in Fig. 18.

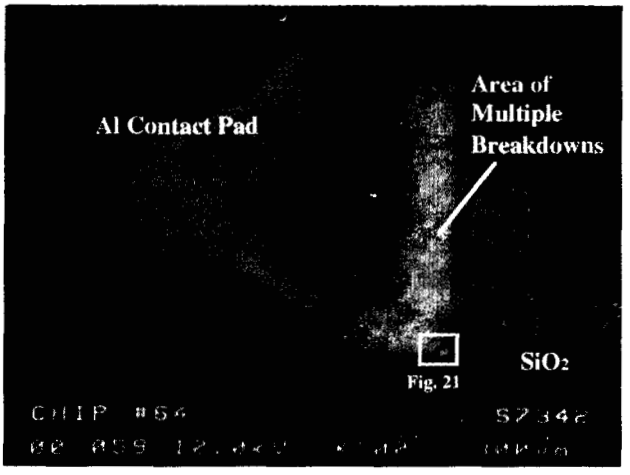

Fig. 20: Multiple Breakdowns for 1 μm Oxide. Note preferred Breakdown Locations on Aluminum Pad Edge and Corner.

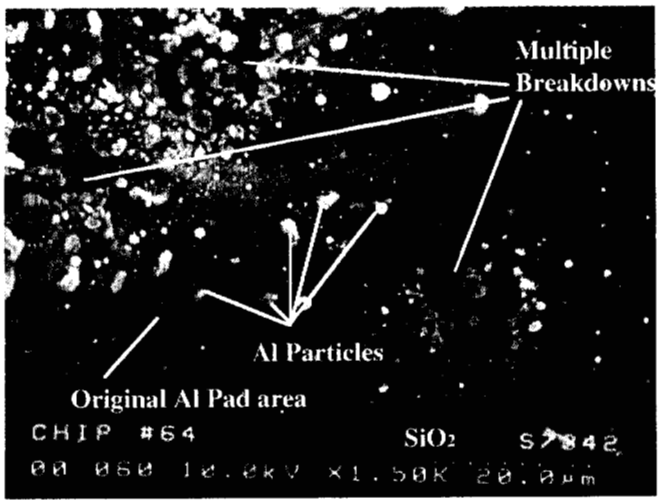

Fig. 21: Close up of Corner Breakdown and Neighboring Breakdowns of Fig. 20.

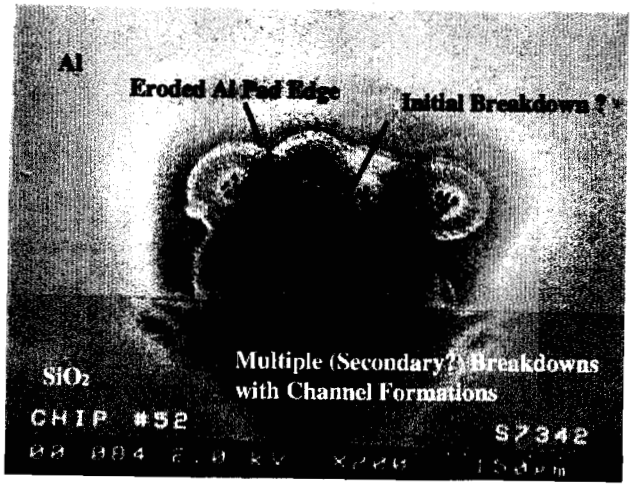

Fig. 22: Multiple Breakdowns for Chip featuring 1.5 μm Oxide. Note Fewer Breakdowns and Start of Channel Formations.

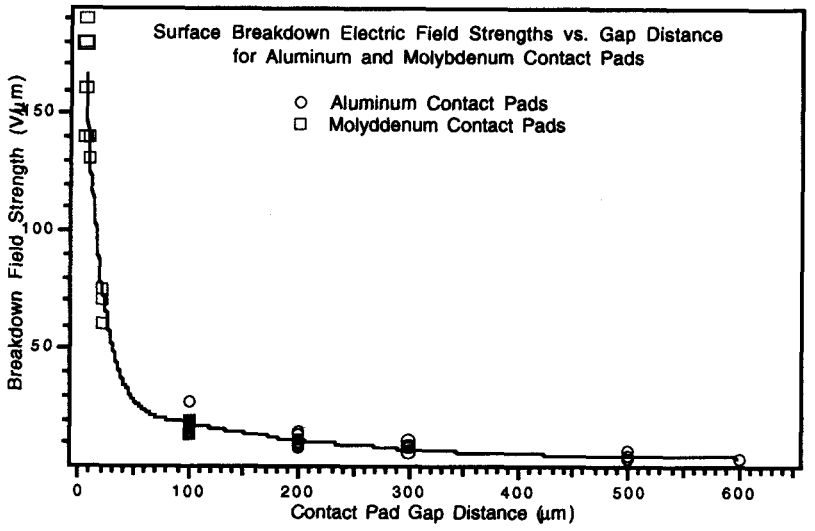

Fig. 23: Surface Breakdown Electric Field Strengths for LTO Oxide using Aluminum and Molybdenum Contact Pads vs. Pad Gap Distance

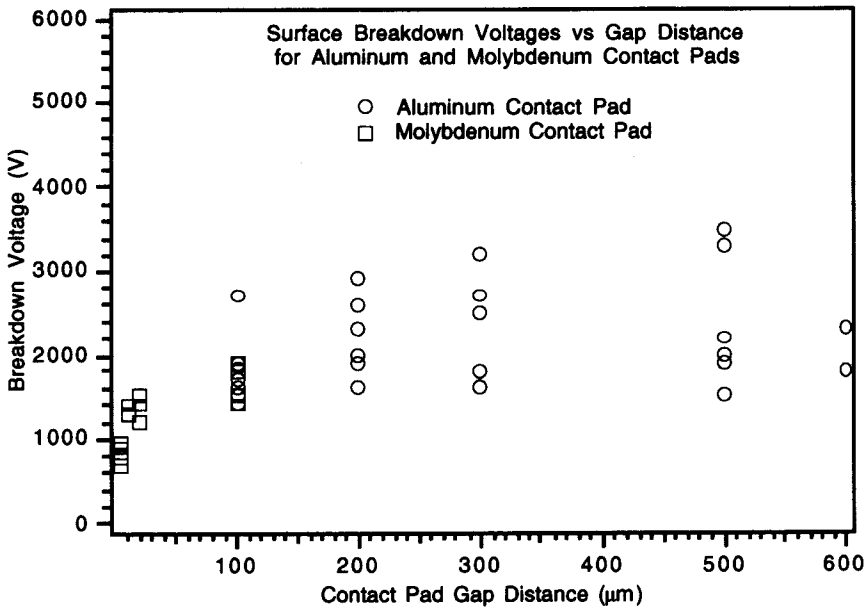

Fig. 24: Surface Breakdown Voltages for LTO Oxides using Aluminum and Molybdenum Contact Pads vs. Pad Gap Distance.

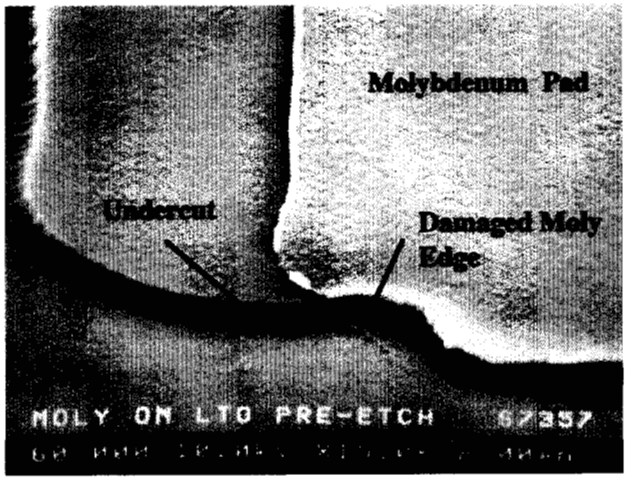

Fig. 25: Photo of Attempt to Achieve Oxide Undercut of Molybdenum Pad

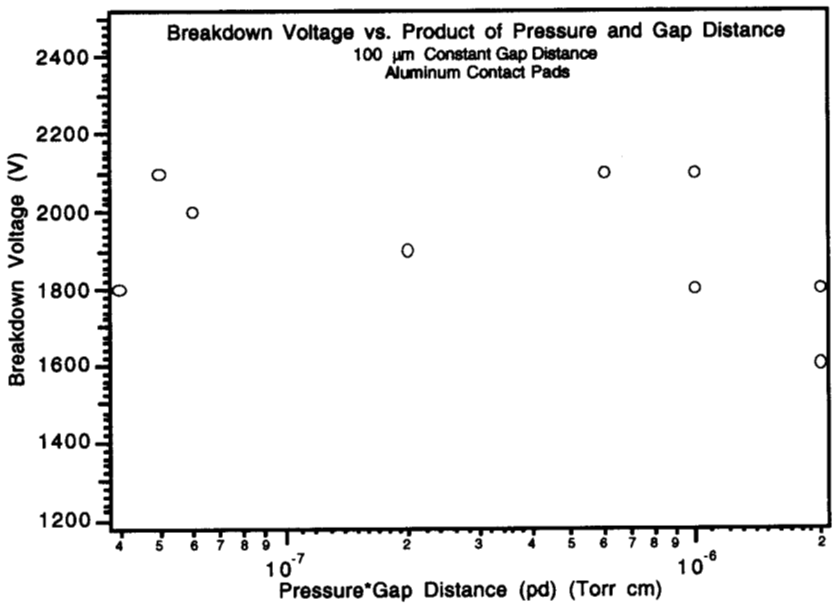

Fig. 26: Breakdown Voltages for Constant Gap Distance at Various Background Pressures

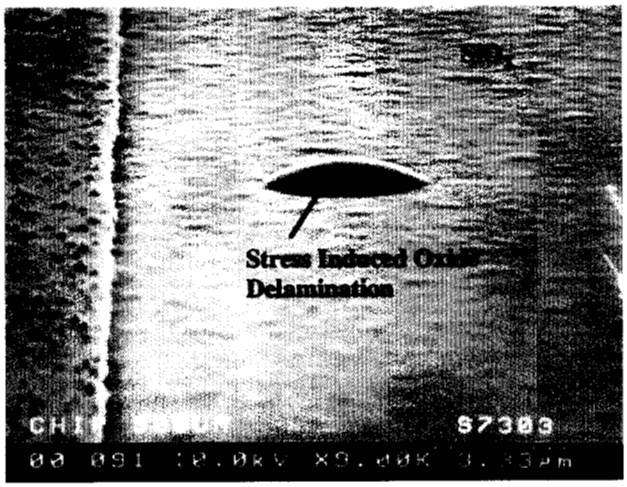

Fig. 27: Example of Stress-Induced Surface Delamination (approx. 3 μm dia.) on Oxide.

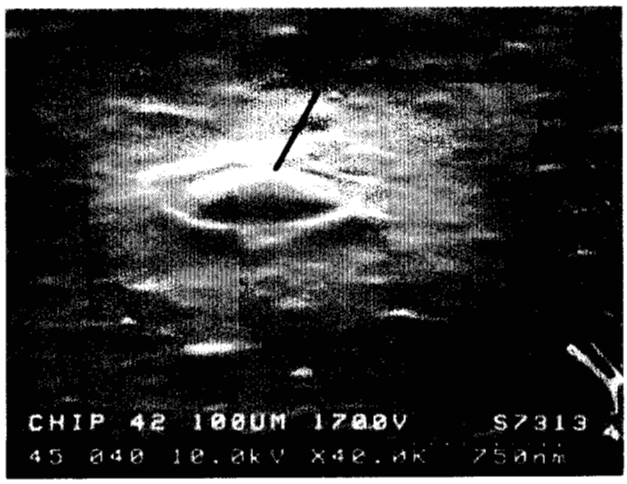

Fig. 28: Example of Stress-Induced Surface Delamination (less than 1 μm dia.) on Oxide.

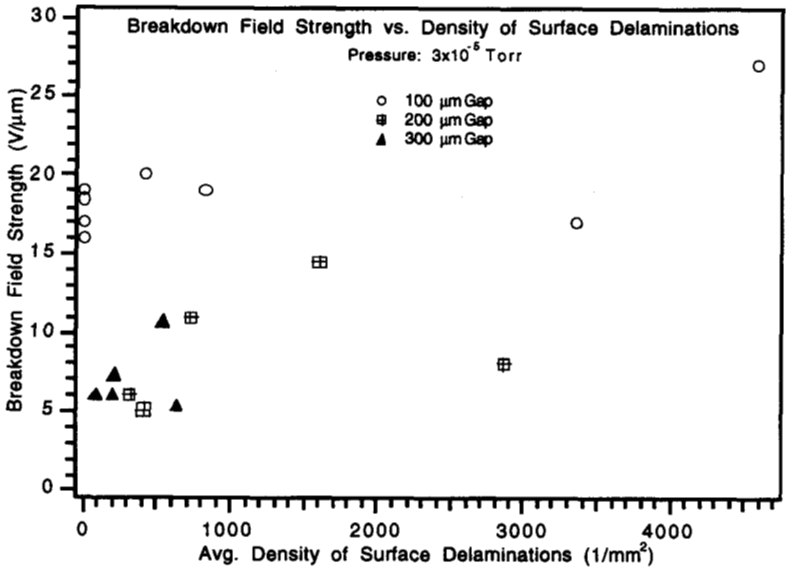

Fig. 29: Breakdown Field Strength vs. Surface Delamination Density

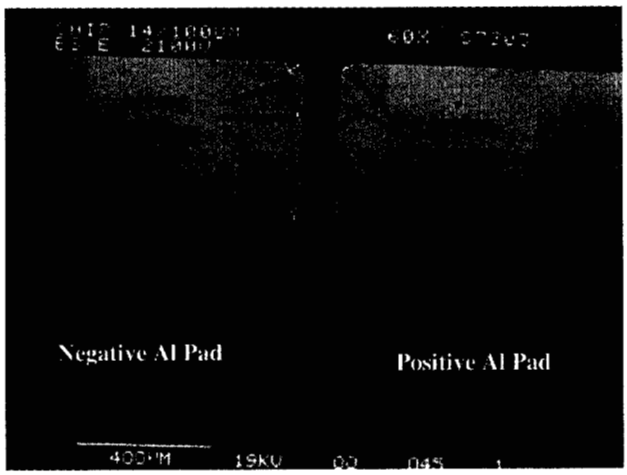

Fig.30: Example of Contact Pad Damage after Surface Arc Breakdown (Arcing Voltage was 2100 V, Gap 100μm)

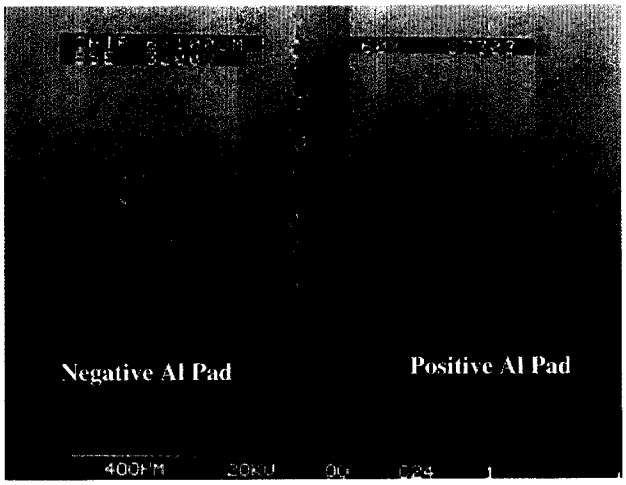

Fig. 31: Example of Contact Pad damage after Surface Arc Breakdown (Arcing Voltage was 3200 V, Gap 100 μm)

Fig.32: Close-up of Aluminum Pad Edge

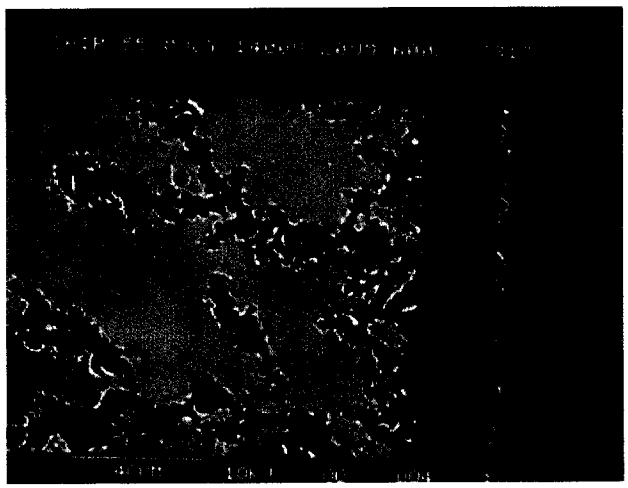

Fig. 33: Post-Test Scan of Molybdenum Surface Breakdown Chip